AMENDMENT TO THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) An information processing apparatus for accessing memory spaces including a user memory space and a secure memory space, comprising:

a general purpose register used for ~~the~~ an arithmetic operation of a CPU and having ~~the~~ a function of receiving, delivering and storing ~~the~~ data, the general purpose register having a data unit;

a secure information unit ~~added to~~ included in the general purpose register and adapted to be set to ~~the~~ a state not requiring security in ~~the~~ a case that ~~where~~ the data is transferred from the user memory space to the data unit of the general purpose register, and adapted to be set to ~~the~~ a state requiring security in ~~the~~ a case that ~~where~~ the data is transferred from the secure memory space to the data unit of the general purpose register;

a data control unit having ~~the~~ a function of determining whether ~~the~~ a value of the secure information unit is in the state requiring security or the state not requiring security when the data of the general purpose register is written in the user memory space, thereby determining whether ~~the~~ a data transfer to the user memory space is prohibited or not; and

an address control unit having ~~the~~ a function of determining which of the user memory space and the secure memory space is indicated by ~~the~~ an address information, and selecting the value of the secure information unit.

2. (Currently Amended) [[An]] The information processing apparatus according to claim 1, further comprising:

a user program arranged in the user memory space;

a secure program arranged in the secure memory space;

an instruction fetch address control unit having ~~the~~ a function of determining which of the user memory space and the secure memory space is indicated by the address information when storing ~~the~~ an instruction code input from the data control unit, and ~~the~~ a function of notifying the data control unit which of the user program and the secure program is under execution; and

an instruction buffer used by the CPU to fetch [[an]] the instruction code and having ~~the~~ a function of storing therein the instruction code input from the data control unit, [[;]]

~~a user program arranged in the user memory space and adapted to be generated mainly by the user; and~~

~~a secure program arranged in the secure memory space and adapted to be generated mainly by the developer, the contents of the secure program being not disclosed to the user;~~

wherein, when the data control unit executes the data transfer from the data unit of the general purpose register to the memory spaces in compliance with a transfer instruction, ~~in such a manner that~~ the data transfer to the user memory space is prohibited, if ~~in the case where~~ the instruction fetch address control unit determines that the instruction code is fetched from the user memory space and the value of the secure information unit indicates ~~is in~~ the state requiring security.

3. (Currently Amended) [[An]] The information processing apparatus according to claim 2, wherein, ~~comprising:~~

the information processing apparatus comprises a plurality of the general purpose registers and ~~used for the arithmetic operation of the CPU, and having the function of receiving and delivering the data from and to the data control unit, and storing the data therein;~~ a plurality

of the secure information units included in each of ~~added to~~ the general purpose registers, respectively, the secure information units further being capable of being set to a ~~and under the control of the address control unit, adapted to be set to selected one of the state requiring security, the state not requiring security and the~~ state of invalid security, [[;]] and

the information processing apparatus further comprises a general purpose register file, the general purpose register file is configured to set, when ~~having such a function that in~~ performing the arithmetic operations between at least two of the general purpose registers in compliance with an operating instruction, the value of the secure information unit of ~~one of~~ the general purpose registers to which ~~for storing~~ ~~the~~ a result of the arithmetic operation is stored ~~is set~~ to the state of invalid security, ~~in the case where~~ if at least one of the values ~~value~~ of the secure information unit ~~of at least one of the general purpose registers~~ indicates that the general purpose register having ~~is in~~ the state requiring security is operated;

wherein, when the data control unit issues ~~an~~ the operating instruction to the general purpose register with the secure information unit having ~~in~~ the state of invalid security, the data control unit prohibits ~~in such a manner as to prohibit~~ the arithmetic operation, if ~~in the case where~~ the instruction fetch address control unit determines that the operating instruction has been fetched from the user memory space.

4. (Currently Amended) [[An]] The information processing apparatus according to claim 2, further comprising a status register used for the arithmetic operation of the CPU and having ~~the~~ a function of holding ~~the~~ a value of ~~the~~ a result of ~~the~~ a comparative arithmetic operation as a comparative flag, the status register further having ~~the~~ a function of keeping ~~the~~ a value of each comparative flag unchanged, when the arithmetic operation is executed between at

least two of the general purpose registers in compliance an operating instruction, if ~~in the case where~~ at least one of the general purpose registers indicates ~~has the value of the secure information unit in~~ the state requiring security ~~at the time of the arithmetic operation executed between at least two of the general purpose registers in compliance an operating instruction~~ and the instruction fetch address control unit determines that the operating instruction has been fetched from the user memory space.

5. (Currently Amended) [[An]] The information processing apparatus according to claim 2, further comprising:

a read/write user IO space used for accessing the user memory space from outside; and

a read/write secure IO space used for accessing the secure memory space from outside, [[;]]

wherein the information processing apparatus is configured to receive an IC card ~~used~~ connectable ~~connected~~ to the secure IO space and having ~~the~~ a function of storing ~~the~~ data, ~~including a debug key therein; and~~ the IC card further including a debug key configured to stop, ~~stored in the IC card and having such a function that~~ when read out by the CPU through the secure IO space when ~~the~~ a developer debugs the secure program with ~~the~~ a user system, ~~the~~ an address determining function ~~of~~ performed by the instruction fetch address control unit and the address control unit ~~is stopped~~;

wherein, when transferring the data from the data unit of the general purpose register to the memory spaces in compliance with the transfer instruction, the data control unit permits ~~has such a function that~~ the data transfer to the user memory space regardless the instruction code is fetched either from the user memory space or the secure memory space, if ~~is not prohibited in the~~

~~case where~~ the debug key is read by the CPU ~~when transferring the data from the data unit of the general purpose register to the memory spaces in compliance with a transfer instruction and at the same time in the case where the instruction is fetched from any one of the user memory space and the secure memory space~~.

6. (Currently Amended) An information processing apparatus for accessing memory spaces including a user memory space and a secure memory space, comprising:

a secure information generating unit for determining which of the user memory space and the secure memory space is indicated by address information, and delivering ~~the~~ data with secure information into a general purpose register with secure information having ~~the~~ a function of receiving and holding the data with secure information;

a built-in RAM space for receiving and holding the data with secure information from the general purpose register and delivering the data with secure information ~~thus~~ held to the general purpose register; and

a data output control unit having ~~the~~ a function of controlling ~~the~~ a data transfer to an external space by using the secure information;

wherein the data output control unit performs ~~the~~ a control operation to determine whether the data transfer to the external space is prohibited or not by ~~the~~ a value of the secure information set in the general purpose register.

7. (Currently Amended) An information processing apparatus for accessing memory spaces including a user memory space and a secure memory space, comprising:

a secure information generating unit for determining which of the user memory space and the secure memory space is indicated by address information, and delivering data with secure information into a general purpose register with secure information having ~~the~~ a function of receiving and holding the data with secure information, and delivering an instruction with secure information into an instruction decoder with secure information having ~~the~~ a function of determining which of the user memory space and the secure memory space is associated with the instruction under execution;

a built-in RAM space with secure information for receiving and holding the data with secure information from the general purpose register and delivering the data with secure information ~~thus~~ held to the general purpose register;

an interrupt saved information unit with secure information having ~~the~~ a function of adding, upon generation of an interrupt process, the secure information of the instruction decoder to ~~the~~ data saved in ~~the~~ a stack area of the built-in RAM space; and

a data output control unit having ~~the~~ a function of controlling ~~the~~ a data transfer to an external space by using the secure information;

wherein the data output control unit performs ~~the~~ a control operation to determine whether the data transfer to the external space is prohibited or not by ~~the~~ a value of the secure information set in the general purpose register.

8. (Currently Amended) An information processing apparatus for accessing memory spaces including a user memory space and a secure memory space, comprising:

a secure information generating unit for determining which of the user memory space and the secure memory space is indicated by address information, and delivering data with secure

information into a general purpose register with secure information having ~~the~~ a function of receiving and holding the data with secure information, and delivering an instruction with secure information into an instruction decoder with secure information having ~~the~~ a function of determining which of the user memory space and the secure memory space is associated with the instruction under execution;

a built-in RAM space with secure information having ~~the~~ a function of receiving and holding the data with secure information from the general purpose register and delivering the data with the secure information ~~thus~~ held to the general purpose register;

an interrupt saved information unit with secure information having ~~the~~ a function of adding, upon generation of an interrupt process, the secure information of the instruction decoder to ~~the~~ data saved in ~~the~~ a stack area of the built-in RAM space;

a stack pointer for defining a part of the built-in RAM space as [[a]] the stack area; and

a saved information rewrite control unit for controlling ~~the~~ a rewrite operation ~~of rewriting~~ in the stack area of the built-in RAM space;

wherein the saved information rewrite control unit prohibits the rewrite operation if ~~in the case where~~ the instruction of the instruction decoder is associated with the user memory space and intended to rewrite the stack area of the built-in RAM space.

9. (Currently Amended) An information processing apparatus for accessing memory spaces including a user memory space and a secure memory space, comprising:

a direct memory access unit (DMA) ~~DMA~~ with secure information having ~~the~~ a function of holding the secure information;

a secure information generating unit for determining which of the user memory space and the secure memory space is indicated by address information, and delivering ~~the~~ data with secure information into the DMA;

a built-in RAM space for receiving and holding the data with secure information from the DMA and delivering the data with secure information ~~thus~~ held to the DMA; and

a data output control unit having ~~the~~ a function of controlling ~~the~~ a data transfer to an external space by using the secure information;

wherein the data output control unit performs ~~the~~ a control operation to determine whether the data transfer to the external space is prohibited or not by ~~the~~ a value of the secure information set in the DMA ~~general purpose register~~.

10. (Currently Amended) An information processing apparatus for accessing memory spaces including a user memory space and a secure memory space, comprising:

a secure information generating unit for determining which of the user memory space and the secure memory space is indicated by address information, and delivering data with secure information into a general purpose register with secure information having ~~the~~ a function of receiving and holding the data with secure information, and delivering an instruction with secure information into an instruction decoder with secure information having ~~the~~ a function of determining which of the user memory space and the secure memory space is associated with the instruction under execution;

an operating unit with secure information having ~~the~~ a function of reflecting the secure information of the instruction decoder in ~~the~~ an arithmetic operation executed in accordance with the instruction decoded by the instruction decoder; and

a data output control unit having ~~the~~ a function of controlling ~~the~~ a data transfer to an external space by using the secure information;

wherein the data output control unit performs ~~the~~ a control operation to determine ~~determined~~ whether the data transfer to the external space is prohibited or not by the secure information set in the general purpose register and the secure information set in the operating unit.

11. (New) The information processing apparatus according to claim 2, wherein

the user program is accessible mainly by a user, and

the secure program is accessible mainly by a developer and contents of the secure program is not disclosed to the user.

12. (New) The information processing apparatus according to claim 1, wherein the data control unit determines whether the data transfer to the user memory space is prohibited or not irrespective of the mode associated with a CPU.

13. (New) The information processing apparatus according to claim 12, wherein the mode associated with the CPU includes a privileged mode or an unprivileged mode.

14. (New) The information processing apparatus according to claim 6, wherein the data control unit determines whether the data transfer to the external space is prohibited or not irrespective of the mode associated with a CPU.

15. (New) The information processing apparatus according to claim 14, wherein the mode associated with the CPU includes a privileged mode or an unprivileged mode.

16. (New) The information processing apparatus according to claim 7, wherein the data control unit determines whether the data transfer to the external space is prohibited or not irrespective of the mode associated with a CPU.

17. (New) The information processing apparatus according to claim 16, wherein the mode associated with the CPU includes a privileged mode or an unprivileged mode.

18. (New) The information processing apparatus according to claim 9, wherein the data control unit determines whether the data transfer to the external space is prohibited or not irrespective of the mode associated with a CPU.

19. (New) The information processing apparatus according to claim 18, wherein the mode associated with the CPU includes a privileged mode or an unprivileged mode.

20. (New) The information processing apparatus according to claim 7, wherein the data control unit determines whether the data transfer to the external space is prohibited or not irrespective of the mode associated with a CPU.

21. (New) The information processing apparatus according to claim 20, wherein the mode associated with the CPU includes a privileged mode or an unprivileged mode.